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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,335	07/24/2003	Vincent J. Jorgensen	X-1251 US	2274

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EXAMINER	
CHUNG, EUN HEE	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,335	JORGENSEN ET AL.	
	Examiner	Art Unit	
	Eun H. Chung	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *6 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Claim Objections

2. Claim 6 and 11 are objected to because of the following informalities:

As per claim 6, "the type of an instance" would be better as " a type of an instance" to avoid any possible antecedent issues.

As per claim 11, " the repeated object" in line 6 would be better as " the repeated objects", and "the modified netlist" in line 15-16 would be better as "a modified netlist".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 3, 9, 16, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 3, 16, and 18, the phrase "regularly" in line 5 renders the claim indefinite because it is unclear what the limitation(s) refers.

Regarding claim 9, the phrase "a repeated listed of root objects" in line 3 renders the claim indefinite because it is unclear what the limitation(s) refers.

5. Claim 6 recites the limitation "the list containing object names for all used instances" in line 5-6. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 11 recites the limitation "all used instances" in line 15. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not

commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 1-13 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joey et al. (US Patent No. 6,345,378), in view of Kuribayashi et al. (US Patent Number 6,374,205).

Regarding Claims 1, 11, 16, and 18,

Joey et al. teaches a method and system of reducing a size of a netlist for a target architecture (Abstract) and machine readable storage (Fig. 1), having stored thereon a computer program having a plurality of code sections executable by a machine (Fig. 1), comprising:

(Claims 1, 11, 16, and 18) create a netlist of objects for the target architecture (Fig. 2, Col. 6 lines 1-51);

(Claims 1, 16, and 18) identify objects specific to the target architecture that are repeated regularly to identify potential dummy objects (Fig. 3-8, Col. 4 lines 46+, Col. 6 lines 33-50, Col. 9 lines 31+, Col. 10 lines 1-33);

(Claim 11) emptying the repeated object found on the list of repeated objects forming a plurality of dummy objects netlist (Fig. 2-9, Appendices A-C, Col. 4 lines 46+, Col. 11 lines 25+, Col. 13 lines 53-65, Col. 14 lines 16-50);

(Claims 1, 16, and 18) create a list of objects used by a predetermined design in the target architecture (Fig. 3-8, Col. 4 lines 46+, Col. 6 lines 33+, Col. 7 lines 1-16, Col. 12 lines 36+, Col. 13 lines 1-52);

(Claims 1, 16, and 18) form a list of unused objects in the target architecture (Fig. 3-7, Col. 4 lines 46+, Col. 6 lines 33-50, Col. 8 lines 50-54, Col. 9 lines 31+, Col. 10 lines 1-33) from the netlist of objects (Fig. 2, Col. 6 lines 1-51) and the list of objects used by the predetermined design (Fig. 2-7, Col. 6 lines 1+, Col. 7 lines 1-16);

(Claims 1, 11, 16, and 18) replace at least one object in the list of unused objects with an appropriate dummy object to form a modified netlist (Fig. 2-9, Appendices A-C, Col. 4 lines 46+, Col. 6 lines 33+, Col. 11 lines 25+, Col. 4 lines 46+, Col. 13 lines 53-65, Col. 14 lines 16-50).

Joey et al. does not teach (Claims 1, 16, and 18) the step of simulating the modified netlist;

(Claim 11) emptying the repeated object found on the list of repeated objects forming a plurality of dummy objects;

(Claim 11) parsing a file to extract a list containing object names for all used objects for the target architecture;

(Claim 11) parsing a netlist of objects line by line for the target architecture;

Kuribayashi et al. teach (Claims 1, 16, and 18) the step of simulating the modified netlist (Abstract, Fig. 1, Col. lines 49-61);

(Claim 11) parsing a file to extract a list containing object names for all used objects for the target architecture (Fig. 3-11, Col. 10 lines 12-29, Col. 11 lines 49+);

(Claim 11) parsing a netlist of objects line by line for the target architecture (Fig. 3-11, Col. 10 lines 12-29, Col. 11 lines 49+);

Joey et al. and Kuribayashi et al. are analogous art because they are both related to a method of reducing circuit data and simulating circuit data.

Therefore, it would have been obvious to one of ordinary skill in the art of at the time the invention was made to include the teachings of Kuribayashi et al., in the method for synthesis shell generation with dummy shell of Joey et al. because simulating the modified netlist, parsing a file to extract a list containing object names for all used instances for the target architecture, and parsing the netlist for the target architecture are well known process in a method of reducing a netlist of circuit. Kuribayashi et al. teach an improved circuit simulating system that provides an accurate reduction and a shortening a simulation time while maintaining the accuracy of simulation (Col. 3 lines 30-59).

Regarding Claim 2,

Joey et al. teach the steps of subtracting the list of objects used by the predetermined design from the netlist of objects (Fig. 2-7, Col. 6 lines 1+, Col. 7 lines 1-16).

Regarding Claim 3,

Joey et al. teach the step of replacing objects in the list of unused objects that are repeated regularly with the appropriate dummy objects to form the modified netlist (Fig. 2-9, Appendices A-C, Col. 4 lines 46+, Col. 6 lines 33+, Col. 11 lines 25+, Col. 4 lines 46+, Col. 13 lines 53-65, Col. 14 lines 16-50).

Regarding Claim 4,

Joey et al. teach the step of replacing each object in the list of unused objects with the object with the appropriate dummy object to form the modified netlist (Fig. 2-9, Appendices A-C, Col. 4 lines 46+, Col. 6 lines 33+, Col. 11 lines 25+, Col. 4 lines 46+, Col. 13 lines 53-65, Col. 14 lines 16-50).

Regarding Claims 5, 7, 17, and 19,

Joey et al. teaches (Claim 7, 17, and 19) forming a modified netlist with the appropriate dummy objects when all lines of the netlist have been parsed (Appendices A-C, Fig. 3-8, Col. 8 lines 50-54, Col. 9 lines 31+, Col. 10 lines 1-33, Col. 11 lines 25+, Col. 14 lines 16-50).

Joey et al. fail to teach (Claims 5, 7, 17, and 19) the steps of parsing a file to extract a list containing object names for all used instances for the target architecture and parsing the netlist for the target architecture line by line.

Kuribayashi et al. teach the steps of parsing a file to extract a list containing object names for all used instances for the target architecture and parsing the netlist for the target architecture (Fig. 3-11, Col. 10 lines 12-29, Col. 11 lines 49+).

It would have been obvious to one of ordinary skill in the art of at the time the invention was made to include Kuribayashi et al.'s steps of parsing a file and the netlist, in the method for simulating the reduced net list generation with dummy shell of Joey et al. because parsing a file to extract a list containing object names for all used instances for the target architecture and parsing the netlist for the target architecture are well known process in a method of reducing a netlist of circuit. Kuribayashi et al. teach an improved circuit simulating system that provides an accurate reduction and a shortening a simulation time while maintaining the accuracy of simulation (Col. 3 lines 30-59).

Regarding Claim 6,

Joey et al. teach the step of replacing the type of an instance for an object found in the repeated list of objects with a type for a corresponding dummy object if the object found in the repeated list is not on the list containing object names for all used instances (Fig. 2-9, Appendices A-C, Col. 4 lines 46+, Col. 6 lines 33+, Col. 11 lines 25+, Col. 4 lines 46+, Col. 13 lines 53-65, Col. 14 lines 16-50).

Regarding Claims 8 and 12,

Joey et al. teach the step of feeding through a signal unchanged () when simulating the appropriate dummy object during a simulation process using the modified netlist (Appendices A-C, Fig. 3-8, Col. 8 lines 50-54, Col. 9 lines 31+, Col. 10 lines 1-33, Col. 11 lines 25+, Col. 14 lines 16-50).

Regarding Claim 9,

Joey et al. teach the step of manually composing a repeated listed of root objects specific to the target architecture (Fig. 2, Col. 5 lines 57-65, Col. 8 lines 55-64, Col. 12 lines 17-44).

Regarding Claims 10, 13, and 20,

Joey et al. teach the step of using a Verilog version (Col. 5 lines 57-67, Col. 14 lines 17-19) and emptying a hardware description language version of a repeated object to form an object devoid of an explicit functional mapping of an input to an output (Fig. 2-9, Appendices A-C, Col. 4 lines 46+, Col. 5 lines 57-67, Col. 6 lines 33+, Col. 11 lines 25+, Col. 4 lines 46+, Col. 13 lines 53-65, Col. 14 lines 16-50).

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joey et al. (US Patent No. 6,345,378), in view of Kuribayashi et al. (US Patent Number 6,374,205), and further in the view of Wirthlin et al. (US Patent Number 6,173,434).

Joey et al. as modified by Kuribayashi et al. teach most all of the instant invention as applied to claims 1-13 and 16-20 above.

Joey et al. as modified by Kuribayashi et al. teach the step of parsing a file containing hierarchical path names (Joey et al.: Appendices A-C, Fig. 4, Col. 7 lines 38-64, Col. 7 lines 2-49, Col. lines 17-50 and Kuribayashi et al.: Fig. 3-11, Col. 10 lines 12-29, Col. 11 lines 49+).

Joey et al. as modified by Kuribayashi et al. fail to teach the memory blocks of a field programmable gate array forming the target architecture.

Wirthlin et al. teach the steps the memory blocks of a field programmable gate array (Abstract, Fig. 2A-2F and 3).

Joey et al. as modified by Kuribayashi et al. and Wirthlin et al. are analogous art because they are both related to a method of simulating circuit data.

Therefore, it would have been obvious to one of ordinary skill in the art of at the time the invention was made to include the teaching of Wirthlin et al. of, in the method for simulating the reduced net list generation with dummy shell of Joey et al. as modified by Kuribayashi et al. because parsing a file to memory blocks of a FPGA is well known process in a method of simulating a circuit data. Wirthlin et al. teach an improved system that provides efficient relocating logic array modules (Abstract, col. 3 lines 39-40, Summary of the Invention).

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joey et al. (US Patent No. 6,345,378), in view of Kuribayashi et al. (US Patent Number 6,374,205), and further in the view of Rupp et al. (US Patent Number 6,857,110).

Joey et al. as modified by Kuribayashi et al. teach most all of the instant invention as applied to claims 1-13 and 16-20 above.

Joey et al. as modified by Kuribayashi et al. teach the step of generating a file containing hierarchical path names (Joey et al.: Appendices A-C, Fig. 4, Col. 7 lines 38-64, Col. 7 lines 2-49, Col. lines 17-50 and Kuribayashi et al.: Fig. 3-11, Col. 10 lines 12-29, Col. 11 lines 49+).

Joey et al. as modified by Kuribayashi et al. fail to teach the converting bitstream names into Verilog hierarchical path names.

Rupp et al. teach the converting bitstream names into Verilog hierarchical path names (Fig 13-16, Col. 16 lines 22+, Col. 17 lines 1-15).

Joey et al. as modified by Kuribayashi et al. and Rupp et al. are analogous art because they are both related to a method of simulating circuit data.

Therefore, it would have been obvious to one of ordinary skill in the art of at the time the invention was made to include the teaching of Rupp et al. of, in the method for simulating the reduced net list generation with dummy shell of Joey et al. as modified by Kuribayashi et al. because the converting bitstream names into Verilog hierarchical path names is well known process in a method of simulating a circuit data. Rupp et al. teach an improved system that incorporates a programmable logic core design and provides signal interface between programmable gate array such as MSA (Abstract, Col. 1 lines 35-55).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Smith et al. disclose routing method in computer aided customization of a two level automated universal array (US Patent No. 4,613,941).

Schmitz et al. disclose a method for allocation of resource in programmable logic device (US Patent No. 5,128,871).

Soughgate et al. disclose computer logic simulation with dynamic modeling (US Patent No. 5,574,893).

Li et al. disclose method for making integrated circuits by inserting buffers into a netlist to control clock skew (US Patent No. 5,638,291).

Yoshinaga et al. disclose semiconductor layout design method (US Pub. No. 2001/0011362).

Ochi et al. disclose circuit simulation with unnecessary circuit disconnected (US Pub. No. 2002/0007261).

Joly et al. disclose timing shell generation through netlist reduction (US Patent No. 5,644,498).

Zahar discloses method for modifying placement of components of an integrated circuit by analyzing resources of adjacent components (US Patent No. 6,434,734).

Kondou discloses method of data processing for designing a semiconductor device (US Patent No. 6,516,457).

Zahar discloses method for forming a structural similarity group from a netlist of an integrated circuit (US Patent No. 6,606,737).

Zahar discloses method for determining control line routing for components of an integrated circuit (US Patent No. 6,687,892).

Dahl et al. disclose method for optimization of the top level in abutted-pin hierarchical, physical design (US Patent No. 6,865,721).

Korobkov discloses method for circuit reduction technique for improving clock net analysis performance (US Patent No. 6,895,524).

Betz et al. disclose techniques for identifying functional blocks in a design that match a template and combining the functional blocks into fewer programmable circuit elements (US Patent No. 6,957,412).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eun H. Chung whose telephone number is 571-272-2164. The examiner can normally be reached on 8:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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7/24/06